WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a plurality of nonvolatile memory cells, each including,

a memory gate electrode formed over a first semiconductor region with first and second gate insulating films interposed therebetween;

first and second switch gate electrodes formed over the first semiconductor region lying on both sides of the memory gate electrode with third gate insulating films interposed therebetween; and

first and second signal electrodes each used a source or drain electrode, which are formed in the first semiconductor region lying in the neighborhood below the respective switch gate electrodes;

wherein the memory gate electrodes and the switch gate electrodes respectively extend in a first direction.

2. The semiconductor device according to claim 1, wherein the first and second signal electrodes respectively have first and second signal wirings which are connected thereto and extend in a second direction substantially orthogonal to the first direction, and the first and second signal wirings are shared between a plurality of nonvolatile memory cells arranged in parallel in the second direction, and the memory gate

electrode and the switch gate electrodes are shared between a plurality of nonvolatile memory cells arranged in parallel in the first direction.

3. The semiconductor device according to claim 2, wherein a pair of the nonvolatile memory cells which is adjacent to the first direction and shares the use of the memory gate electrode, is configured so that either one of the first and second signal electrodes is used in common and the others thereof are individualized, and the first and second signal electrodes are connected to their corresponding first and second signal wirings.

4. The semiconductor device according to claim 3, wherein the single nonvolatile memory cell is capable of storing 2-bit information therein according to a first state in which carriers are captured on the first switch gate electrode side of the second gate insulating film, a second state in which the carriers captured in the first state are reduced, a third state in which carriers are captured on the second switch gate electrode side of the second gate insulating film, or a fourth state in which the carriers captured in the third state are reduced.

5. The semiconductor device according to claim 3, wherein the first semiconductor region is a well region, a plurality of the nonvolatile memory cells, which share

the use of the memory gate electrode and the first and second switch gate electrodes, are disposed in a plurality of electrically-separated well regions in divided form, and each of the nonvolatile memory cells discharges carriers from the second gate insulating film to the corresponding well region according to the difference in potential between the well region and the memory gate electrode.

6. The semiconductor device according to claim 3, wherein the nonvolatile memory cell discharges carriers from the second gate insulating film to the first semiconductor region according to the difference in potential between the first or second signal electrode selected by the first or second switch gate electrode and the first semiconductor region.

7. The semiconductor device according to claim 3, wherein the nonvolatile memory cell discharges carriers from the second insulating film to the memory gate electrode according to the difference in potential between the corresponding signal electrode selected by the first or second switch gate electrode and the memory gate electrode.

8. The semiconductor device according to claim 3, wherein high-concentration impurity regions are

respectively formed in the first semiconductor region placed below the first and second gate insulating films with widths less than or equal to width sizes of the corresponding insulating films.

9. The semiconductor device according to claim 8, wherein when the carriers are captured on the first switch gate electrode side or second switch gate electrode side of the second gate insulating film, the first semiconductor region is supplied with a backward substrate bias voltage.

10. The semiconductor device according to claim 4, wherein when a potential at the second signal electrode selected by the second switch gate electrode is set higher than a potential at the first signal electrode selected by the first switch gate electrode, the nonvolatile memory cell reads 1-bit storage information placed in the first or second state, and when a potential at the first signal electrode selected by the first switch gate electrode is set higher than a potential at the second signal electrode selected by the second switch gate electrode, the nonvolatile memory cell reads 1-bit storage information placed in the third or fourth state.

11. The semiconductor device according to claim 1, wherein a first signal wiring is connected to the first

signal electrode of the nonvolatile memory cell, a second signal wiring is connected to the second signal electrode of the nonvolatile memory cell, and

further including a precharge circuit capable of precharging the first signal wiring and the second signal wiring, a sense amplifier which detects a change in the level of the first signal wiring, and a control circuit, and

wherein the control circuit allows the precharge circuit to perform a precharge operation so that either one of the first and second signal electrodes and the other thereof are respectively brought to a high potential and a low potential according to a read address and causes the sense amplifier to detect the presence or absence of a change in the level of the first signal wiring after the completion of the precharge operation.

12. A semiconductor device comprising:

a plurality of nonvolatile memory cells provided in a first semiconductor region formed on a semiconductor substrate,

said each nonvolatile memory cell including,

first and second gate insulating films laminated on the first semiconductor region;

a memory gate electrode formed over the first and second gate insulating films;

first and second switch gate electrodes

formed over the first semiconductor region lying on both sides of the memory gate electrode with third gate insulating films interposed therebetween; and

first and second signal electrodes each used a source or drain electrode, which are formed in the first semiconductor region lying in the neighborhood below the respective switch gate electrodes;

wherein the second insulating film comprises silicon nitride;

wherein the memory gate electrode comprises polycrystalline silicon corresponding to a first layer;

wherein the first and second switch gate electrodes respectively comprise polycrystalline silicon corresponding to a second layer;

wherein the memory gate electrode and the first and second switch gate electrodes extend in a first direction; and

wherein first and second signal wirings respectively connected with the first and second signal electrodes extend in a second direction substantially orthogonal to the first direction.

13. A semiconductor device comprising:

a plurality of nonvolatile memory cells provided in a first semiconductor region formed on a semiconductor substrate,

said each nonvolatile memory cell including,

first and second gate insulating films laminated on the first semiconductor region;

a memory gate electrode formed over the first and second gate insulating films;

first and second switch gate electrodes formed over the first semiconductor region lying on both sides of the memory gate electrode with third gate insulating films interposed therebetween; and

first and second signal electrodes each used a source or drain electrode, which are formed in the first semiconductor region lying in the neighborhood below the respective switch gate electrodes;

wherein the second insulating film comprises silicon nitride;

wherein the switch gate electrodes respectively comprise polycrystalline silicon corresponding to a first layer;

wherein the memory gate electrode comprises polycrystalline silicon corresponding to a second layer;

wherein the memory gate electrode and the first and second switch gate electrodes extend in a first direction; and

wherein first and second signal wirings respectively connected with the first and second signal electrodes extend in a second direction substantially orthogonal to the first direction.

14. The semiconductor device according to claim 13, wherein a memory circuit provided with the nonvolatile memory cells as storage elements, a CPU capable of accessing the memory circuit, and an external interface circuit connected to the CPU are provided on a single semiconductor chip.

15. An IC card comprising:

a card substrate;

a semiconductor device according to claim 14; and

a card interface terminal connected to the external interface circuit of the semiconductor device, all of which being provided on the card substrate.

16. An IC card comprising:

a card substrate;

a semiconductor device according to claim 14;

a high-frequency interface circuit connected to the external interface circuit of the semiconductor device; and

an antenna connected to the high-frequency interface circuit, all of which being provided on the card substrate.

17. A method of manufacturing a semiconductor device, comprising the steps of:

forming a first conductivity type first

semiconductor region on a main surface of a semiconductor substrate;

forming a first insulating film and a second insulating film on the main surface of the semiconductor substrate on the first semiconductor region in order;

forming a first conductor element having a first width as viewed in a first direction of the main surface of the semiconductor substrate and a second width as viewed in a second direction substantially orthogonal to the first direction, on the second insulating film;

introducing a first impurity of the first conductivity type into the first semiconductor region below the first conductor element as viewed in the first direrction to selectively form second semiconductor regions;

forming a third insulating film on side walls of the first conductor element as viewed in the first direction;

forming second and third conductor elements respectively having a third width as viewed in the first direction and a fourth width as viewed in the second direction at both ends of the first conductor element as viewed in the first direction with the third insulating film interposed therebeween; and

introducing a second impurity of a second conductivity type opposite to the first conductivity type as viewed in the first direction to form a third

semiconductor region within the first semiconductor region on the sides opposite to the first conductor element, of the second and third conductor elements;

18. The method according to claim 17, wherein said second semiconductor region forming step further includes the step of introducing a third impurity of the second conductivity type into the first semiconductor region at both ends of the first conductor element, the third impurity is ion-implanted at a first angle to the main surface of the semiconductor substrate, the first impurity is ion-implanted at a second angle to the main surface of the semiconductor substrate, and the first angle is larger than the second angle.

19. The method according to claim 17, wherein the second width of the first conductor element is greater than the first width, the fourth width of the second conductor element is greater than the third width, and the first and second conductor elements extend in the second direction.

20. The method according to claim 17, wherein the first insulating film comprises silicon oxide, and the second insulating film comprises silicon nitride.

21. A method of manufacturing a semiconductor

device, comprising the steps of:

forming a first conductivity type first semiconductor region on a main surface of a semiconductor substrate;

forming two first conductor elements having a first width as viewed in a first direction of the main surface of the semiconductor substrate and a second width as viewed in a second direction substantially orthogonal to the first direction, on the first semiconductor region with a predetermined interval interposed therebetween;

forming a first insulating film on side walls of the first conductor element in a region between the first conductor elements;

introducing a first impurity of the first conductivity type within the first semiconductor region in the region lying between the first conductor elements and interposed by the first insulating film formed on the side walls of the first conductor element in order to form a second semiconductor region therewithin;

forming a second insulating film and a third insulating film over the surface of the semiconductor substrate in the region between the first conductor elements;

forming a second conductor element having a third width as viewed in the first direction and a fourth width as viewed in the second direction, on the third insulating film; and

introducing a second impurity of a second conductivity type opposite to the first conductivity type as viewed in the first direction to form a third semiconductor region within the first semiconductor region on the side opposite to the second conductor element, of the first conductor element.

22. The method according to claim 21, wherein said first insulating film forming step includes the step of depositing an insulating film on the semiconductor substrate, and the step of subjecting the insulating film to anisotropic etching and selectively leaving the insulating film on the side walls of the first conductor element.

23. The method according to claim 21, wherein the second conductor element is formed on the side walls of the first conductor element with the third insulating film interposed therebetween.

24. The method according to claim 23, wherein the second insulating film comprises silicon oxide, and the third insulating film comprises silicon nitride.

25. The method according to claim 21, wherein the second width of the first conductor element is greater than the first width, the fourth width of the second

conductor element is greater than the third width, and the first and second conductor elements extend in the second direction.

26. A semiconductor apparatus comprising:

a nonvolatile memory; and

a central processing unit,

wherein said nonvolatile memory has a plurality of memory cells,

wherein each of said memory cells includes:

a memory gate formed over a first semiconductor region with a first insulating film and a second insulating film interposed therebetween;

a first switch gate formed over said first semiconductor region to a first side of said memory gate with a third insulating film;

a second switch gate formed over the first semiconductor region to a second side of said memory gate with a fourth insulating film, wherein said second side is opposite said first side across said memory gate; and

a second semiconductor region and a third semiconductor region respectively formed adjacent to opposite sides of said first semiconductor region; and

wherein said first nonvolatile memory is capable of storing a program and data, and

wherein said central processing unit executes said program read from said first nonvolatile memory.

27. A semiconductor apparatus according to claim 26, further comprising a random access memory,

wherein said random access memory is used for a work memory for said central processing unit.

28. A semiconductor apparatus according to claim 27, wherein said central processing unit controls to access to said nonvolatile memory.

29. A semiconductor apparatus according to claim 28, wherein said nonvolatile memory is capable of rewriting data stored therein.

30. A semiconductor apparatus according to claim 29, further comprising a second nonvolatile memory,

wherein said central processing unit controls to access to said second nonvolatile memory.

31. A semiconductor apparatus according to claim 29, further comprising a communication circuit and an antenna,

wherein said communication circuit couples to said antenna, and

wherein said communication circuit is capable of communication by electromagnetic induction.

32. A semiconductor apparatus according to claim 26, wherein each said memory cell is capable of storing data by trapping electrons in said memory gate thereof to change a threshold voltage.